AMENDMENT TO THE SPECIFICATION:

Please amend paragraph [0037] as follows:

The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in FIG. 5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in FIG. 5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4.times.3 interconnect pads 21, arranged in a first row, a second row, a third row, a first column, a second column, a third column, and a forth column. The I/O cell is, for example, a single group including a single unit having one or more input-output buffers formed in the chip 13 and an S-terminal (signal line terminal), a V-terminal (power source terminal) and a G-terminal (ground terminal) connected to the input-output buffers, or the single I/O cell may include only the S-terminal. However, the number of the terminals and the arrangement are not restricted to the above, and an I/O cell having an arbitrary array can be formed.

Please amend paragraph [0047] as follows:

In view of the increased number of layers (two-layered) of the interconnect lines 22a, 22b, as schematically shown in FIG. 8, the grouped I/O cell in the arrangement of the interconnect pads 21 as well as the ball electrodes 31 of the chip 13 can be divided into a first I/O cell (CELL-

1) and a second I/O cell (CELL-2). Part of the first I/O cell (CELL-1 or a first group of I/O cells) or I/O cells (CELL-1A) are disposed on the outer peripheral region of the chip 13, arranged in a first row and a first column, and the remaining I/O cells (CELL-1B) are disposed on the inner sections of the chip 13, arranged in a second row and a second column. Intervals are secured between the first I/O cells (CELL-1A) remaining on the outer periphery for passing the interconnect lines 22 drawn from the inner I/O cells (CELL-1B). In FIG. 8, the first I/O cells (CELL-1) disposed on the outer periphery are alternately disposed on outer sections (CELL-1A) and inner parts (CELL-1B) in the outer periphery. The second I/O cells (CELL-2 or a second group of I/O cells) are disposed on the sections inside of the other I/O cells (CELL-1), and part of the second I/O cell (CELL-2) or I/O cells (CELL-[[2B]]2A) are disposed inside of the remaining I/O cells (CELL-[[2A]]2B), the Cell-2B being arranged in a third row and a third column and the and the Cell-2A being arranged in a forth row and a forth column and intervals are secured between the outer second I/O cells (CELL-2A) for passing the interconnect lines drawn from the inner second I/O cells (CELL-2B). In FIG. 8, similarly to the first I/O cells (CELL-1), the second I/O cells (CELL-2) are alternately disposed on outer sections (CELL-2A) and inner parts (CELL-2B).